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PATENT NUMBER and
ISSUE DATE

U.S. UTILITY Patent Application

| APPL NUM | FILING DATE | CLASS | SUBCLASS | GAU | EXAMINER |
|----------|-------------|-------|----------|------|-----------|
| 10052519 | 01/23/2002 | 365 | 185.9 | 2818 | H.O. HCAI |

**APPLICANTS: Hirano Yasuaki;

**CONTINUING DATA VERIFIED:

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** FOREIGN APPLICATIONS VERIFIED:

JAPAN 2001-054270 02/28/2001

| | | |
|---|--|----------------------------------|
| PG-PUB | DO NOT PUBLISH <input type="checkbox"/> | RESCIND <input type="checkbox"/> |
| Foreign priority claimed | <input type="checkbox"/> yes <input type="checkbox"/> no | ATTORNEY DOCKET NO |
| 35 USC 119 conditions met | <input type="checkbox"/> yes <input type="checkbox"/> no | 204552022100 |
| Verified and Acknowledged Examiners's initials | | |
| TITLE : Nonvolatile semiconductor memory device capable of preventing occurrence of latchup | | |

U.S. DEPT. OF COMM./PAT. & TM.-PTO-436L (Rev. 12-94)

| NOTICE OF ALLOWANCE MAILED | | CLAIMS ALLOWED | |
|---|-----------|----------------------|----------------------|
| | | Total Claims | Print Claim for O.G. |
| Assistant Examiner | | DRAWING | |
| ISSUE FEE | | Sheets Drwg. | Figs. Drwg. |
| Amount Due | Date Paid | Print Fig. | |
| Primary Examiner | | Application Examiner | |
| <input type="checkbox"/> TERMINAL DISCLAIMER | | PREPARED FOR ISSUE | |
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